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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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09/613,331

07/07/2000

MASAMOTO TAGO

WN-2205

9072

466

7590

08/28/2002

YOUNG & THOMPSON
745 SOUTH 23RD STREET 2ND FLOOR
ARLINGTON, VA 22202

EXAMINER

HOANG, QUOC DINH

ART UNIT

PAPER NUMBER

2818

DATE MAILED: 08/28/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/613,331

Applicant(s)

TAGO ET AL.

Examiner

Quoc D Hoang

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on the RCE filed on 7/29/2002.
- 2a) ☐ This action is FINAL.
- 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,2,6,7 and 9-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2,6,7 and 9-23 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 6.

- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

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DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under Ex Parte Quayle, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114.

Applicant's submission filed on 7/29/02 has been entered.

Information Disclosure Statement

2. The Information Disclosure Statement filed on 7/03/02 and 7/29/02 has been considered.

Allowable Subject Matter

3. The indicated allowability of claims 1, 2, 6, 7 and 9-23 is withdrawn in view of the newly discovered reference(s) to Saitou et al. Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-2, 6, 7 and 9-23 are rejected under 35 U.S.C. 102(b) as anticipated over Saitou et al. (U.S. Patent No. 5,162,240).

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Regarding claims 1, 2, 6, 9, 12-17, 19 and 23, Saitou et al., Figures. 1-13, and related text on col. 1-20 which discloses a method of manufacturing a system semiconductor device comprising: forming a system LSI cell portion 30 which includes a plurality of functional blocks for realizing specific functions which serve as a unit circuits and realize specific function on a semiconductor chip (col. 16, lines 1-55 and col.20, lines 50-51 and Fig. 13); forming a global wiring layer 20 by forming a wiring layer on a semiconductor substrate (col. 15, lines 38-67 and col.16, lines 1-50 and Figs. 12-13); laminating the system LSI cell portion 30 with the global wiring layer 20 such that the functional blocks are electrically connected to each other (col. 15, lines 38-67 and col.16, lines 1-50 and Figs. 12-13) wherein the global wiring layer 20 is formed by sequentially laminating a first wiring layer 16X, a second wiring layer 16Y, an insulating layer 16I, and inner bumps 23 on a semiconductor substrate 10 (col. 15, lines 38-67 and col.16, lines 1-50 and Figs. 12-13).

Regarding claims 7, 9, 18 and 20, Saitou et al., discloses the insulting layer 16I includes a via which electrically connects the first wiring layer 16X with the second wiring layer 16Y (Fig. 12).

Regarding claim 10 and 21, Saitou et al., discloses the global wiring layer 20 has at least one or more of the wiring layers (Figure. 13).

Regarding claims 11 and 22, Saitou et al., discloses the global wiring layer 20 has at least one or more of the insulating layers (Figure. 13).

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6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quoc Hoang whose telephone number is (703) 306-5795. The examiner can normally be reached on Monday -Friday from 8.00 AM to 5.00 PM.

If attempt to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms., can be reached on (703) 308-4910.

Quoc Hoang
Patent Examiner/AU 2818



David Nelms
Supervisory Patent Examiner
Technology Center 2800